NASA TECH BRIEF

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Silicon Switching Transistor with High Power and Low Saturation Voltage

The problem:

To construct a silicon power-transistor that has low electrical resistance and low thermal impedance.

The solution:

An assembly of two individually encapsulated silicon-chip transistors.

How it's done:

Each encapsulated chip is a disc-shaped hermetically-sealed package with the emitter connected to one side and the collector to the opposite side. The use of two individual chips permits close matching of performance and ease of replacement should one unit fail. Electrical resistance and thermal impedance are low because of short lead lengths, and the external contact surfaces are plated to reduce resistance at the interfaces. Both units are mounted to the same heat sink so that their temperatures will most probably be equal. Since each unit is individually capable of carrying the rated current, emitter ballast resistors (which might increase saturation voltage) are not required; current sharing is assured because the chips are matched.

A compression-bond—encapsulation technique is used for contacting the collector, base, and emitter of the basic transistor fusion. The emitter and collector contact faces of the unit are identical, and therefore interchangeable, which makes possible use of a mounting in which the emitters are directly in contact with a grounded heat sink. A commercially available aluminum heat sink may be used. A narrow profile offers advantages in electrical resistance, thermal resistance, and lead wire inductance. The insulated base lead passes through a pressure contact and makes contact to the weld flange of the emitter seal.

The top portion of the assembly is a copper collector-contact bar which provides a low-resistance contact to the collector of the units. Since the thermal conductivity of copper is about twice that of aluminum, heat is conducted to the heat sink much faster and over a much larger area than if the devices were mounted directly on the heat sink. The units are located on the collector contact bar, and an emitter contact bar is located on the emitter contact area of the flat package. The top compression bar is located and held in position over the emitter contact bar by two dowel pins which fit in a milled groove on both the emitter and top bars. Alignment of the assembly is accomplished by a compression bolt and insulator. The required force on the units is maintained by the bolt along with the compression nut and Belleville springs; the force required to provide low thermal and electrical resistance is about 900 kg (2000 lbs).

Notes:

1. The following documentation may be obtained from:
   National Technical Information Service
   Springfield, Virginia 22151
   Single document price $6.00
   (or microfiche $0.95)
   Reference: NASA CR-112870 (N70-36859), Design and Development of a High Power, Low Saturation Voltage, Multi-Chip Switching Transistor.

Patent status:

NASA has decided not to apply for a patent.

(continued overleaf)

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